A New Approach to the RF Power Operation of MESFET's

GEORGE HALKIAS, HENRI GERARD, YVES CROSNIER, AND GEORGES SALMER

Abstract—**A new numerical large-signal model for a MESFET is described which allows investigations of the behavior of these devices at *X*-band frequencies under large-signal conditions. The results of the numerical simulations are compared with those of the measurements and provide an improved understanding of the behavior of GaAs MESFET's that operate at microwave frequencies and with high power requirements. Furthermore, our analysis yields some indications about the optimum design of these devices.**

NOMENCLATURE

a	Thickness of the active layer.
E_x	Longitudinal component of the electric field into the channel at abscissa x.
I_{d0}	Drain bias current.
J_x	Current density at abscissa x.
m^*	Effective mass of the electrons.
N_d	Donor density per unit volume.
n_x	Electron density at abscissa x.
P_e	Input power.
q	Electron charge.
V_{ds0}	Drain–source bias voltage.
V_{g0}	Gate–source bias voltage.
v_x	Electron velocity.
W_x	Electron energy at abscissa x.
Y_x	Undepleted portion of the active layer at abscissa x.
Z	Total width of the device.
Z_L	Load impedance.
ϵ	Permittivity of GaAs.
ρ_x	Charge density at abscissa x.

I. INTRODUCTION

THE GREAT progress in MESFET technology achieved over the last 15 years has allowed the fabrication of power MESFET's which operate with satisfactory performance in *X*-band and beyond. The continued development of these devices has been realized by employing experimental and empirical processes and by theoretical investigations.

Manuscript received June 11, 1988; revised November 28, 1988.

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IEEE Log Number 8926586.

The models proposed to describe the power RF behavior of the MESFET's are based on equivalent circuit models (see, for instance, [1] and [2]). Exceptions to this approach are very few (see the work by Madjar *et al.* [3], who use the classical physical equations to describe the behavior of the intrinsic device).

It is well established that the "hard" limits for the output signal in large-signal operation are the "natural" limits of static output characteristics, i.e., 1) knee voltage V_{dt}, 2) cutoff region, 3) breakdown voltage V_{br}, and 4) maximum output current I_{dss}. Thus, in conventional class A operation, i.e., when the bias conditions are $V_{ds0} = (V_{br} - V_{dt})/2 + V_{dt}$ and $I_{d0} = I_{dss}/2$, and assuming a resistive load $R_L = (V_{br} - V_{dt})/I_{dss}$, the maximum available output power delivered at R_L must be $P_{\max} = 1/8 \times (V_{br} - V_{dt}) \times I_{dss}$.

However, Snider has proved [4], with low-frequency considerations, that a unilateral RF power amplifier can deliver 1.62 times the above classical class A value of output power. This is achieved by overdriving the amplifier; hence the output signal approaches that of a square waveform.

The question arising from this discussion is, Is it possible to obtain a similar performance at the *X*-band frequencies? A first obvious "response" is that the assumption of a pure resistive load is not the best choice for these frequencies. In fact, at *X*-band frequencies with small-signal operation, we expect that the matching load impedances would be very "reactive" and thus that the instantaneous output current versus the instantaneous output voltage (namely, the dynamic diagram of operation) would be an ellipse (assuming that there is no distortion). The major axis of this ellipse makes an angle θ with the voltage axis, as in Fig. 1. This angle θ depends only on the real and the imaginary part of the load impedances (R and X, respectively). Moreover, Fig. 1 demonstrates the dependence of θ on R and X at a I_{ds}–V_{ds} frame in which the unit of length on the voltage axis corresponds to 1 V and the unit of length on the current axis corresponds to 10 mA.

However in large-signal operation it is not so easy to say what happens to the dynamic diagram of operation and to the ellipse that corresponds to the fundamental frequency (and which is the carrier of output available power P_s). At this point we should note the remarkable finding of Tucker

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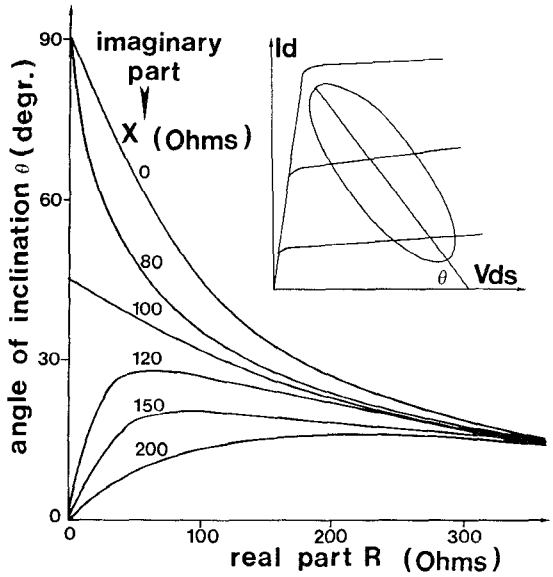

Fig. 1. Angle θ between the major axis of the ellipse (corresponding to the linear RF operation of the transistor) and the voltage axis of the static output characteristics, as a function of the real part (R) and the imaginary part (X) of the load impedance.

[5], who demonstrated that for large-signal operation the optimum load impedance is not the complex conjugate of the large-signal output impedance.

In this paper we will attempt to answer these questions and, in general, to investigate the physical behavior of the MESFET when it operates under large-signal conditions. Nevertheless, modeling the microwave power operation of a MESFET by using the physical transport equations is a complex procedure and precludes the use of full two-dimensional models because of the excessive computer time required for numerical simulations of this kind. Thus, we chose a quasi-two-dimensional model of the type developed in a static version by Cappy [6], [7]. In addition, we used a load-pull method [8] to perform the RF measurements for a MESFET test and thus to compare the experimental data with the results of the numerical simulations.

In Section II we describe the dynamic model for the intrinsic device along with the environment of the parasitic elements, and in Section III we present the results of numerical simulations and of experimental measurements.

II. The Model

Our quasi-two-dimensional dynamic model takes into account the nonstationary electron dynamics by using a simplified form of relaxation equations. In addition, the avalanche breakdown phenomenon is modeled with an empirical approach.

Fig. 2 shows a cross section of the device structure. The basic assumptions used for the construction of the model are:

- the doping profile in the active layer is uniform in the y direction;
- the depletion region is completely empty of carriers;

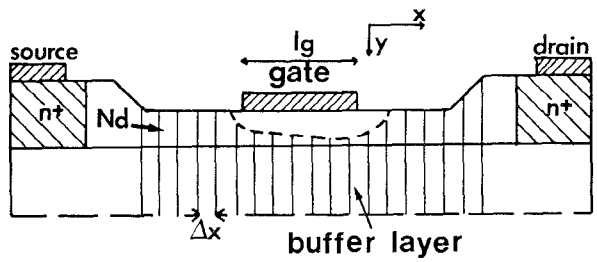

Fig. 2. Cross-sectional view of a MESFET structure.

- the component E_y of the electric field into the channel is assumed to be zero;
- the diffusion of carriers is negligible.

The transport properties of the electrons in the device are described by the following equations, expressed in discrete form:

1) Poisson's equation into the channel:

$$\frac{E_x - E_{x-1}}{\Delta x} = \frac{\rho_x}{\epsilon} \tag{1}$$

where $\rho_x = q(n_x - N_d)$.

2) Continuity equation, applied to the volume element $a \times Z \times \Delta x$:

$$\frac{J_x - J_{x-1}}{\Delta x} + \frac{\rho_{t,x} - \rho_{t-1,x}}{\Delta t} = 0 \tag{2}$$

where $\rho_{t,x}$ is the charge density at the abscissa x and at time t.

3) The particle current equation is given by

$$I_x = q \times n_x \times v_x \times Y_x \times Z \tag{3}$$

where Y_x is the total height of the channel at the abscissa x, i.e., the remaining undepleted portion of the active layer plus the equivalent effective penetration Y_{bx} of the carriers into the buffer layer defined below.

4) Equations of the balance of the momentum and energy [9], [10]:

$$\frac{v_x - v_{x-1}}{\Delta x} = \frac{qE_x}{v_x m^*(W)} - \frac{1}{\tau_p(W)} \tag{4}$$

$$\frac{W_x - W_{x-1}}{\Delta x} = qE_{x-1} - \frac{W_x - W_0}{v_{x-1}\tau_w(W)} \tag{5}$$

where $\tau_p(W)$ and $\tau_w(W)$ are the momentum and energy relaxation times, respectively. Their dependence on electron energy is obtained by Monte Carlo calculations [11], [12].

5) The current injection into the buffer layer is taken into account by using the following equation, which gives the effective injection depth Y_{bx} into the buffer layer [13]:

$$Y_{bx} = Y_s\left(1 - \frac{N_d}{n_x}\right) \tag{6}$$

where the constant $Y_s \approx l_g/2 + a$.

In addition, we calculated the shape of the depletion region point by point into the channel by applying Gauss's law at each volume element. The fringing on both sides of the gate is deduced from a two-dimensional model [14].

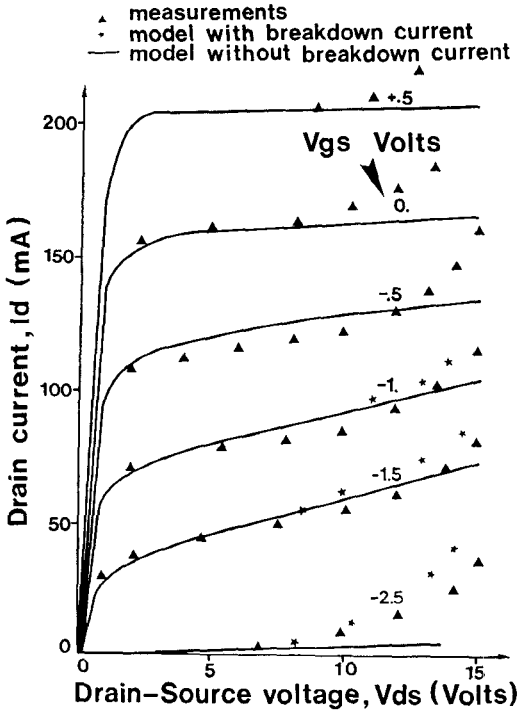

Fig. 3. Simulated and measured $I-V$ static output characteristics of the device.

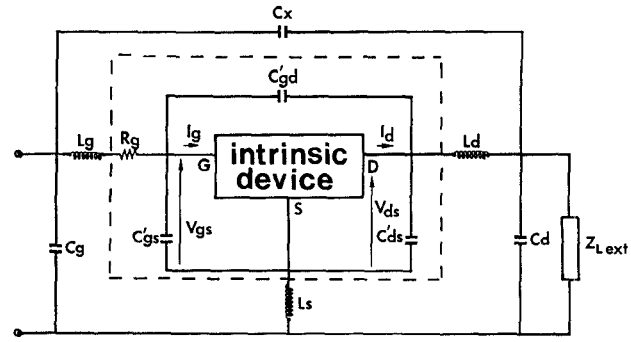

Fig. 4. Equivalent circuit of the parasitic element environment of the intrinsic device.

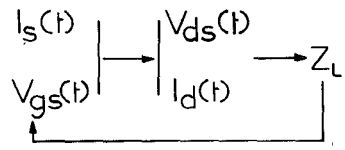

Fig. 5. Simplified diagram for the dynamic model.

Equations (1)–(4) and (6) form a linear system that can be solved using the classical numerical routines. Equation (5) is used to calculate the energy of the electrons and then to obtain $\tau_w(W)$ and $\tau_p(W)$.

Starting from the source contact with appropriate boundary conditions we advanced point by point towards the drain contact; this procedure was repeated for all the points on a period.

It has been mentioned in Section I that the breakdown voltage is one of the factors which limit the output power of a MESFET. In particular, the avalanche breakdown is the mechanism that dominates the pinch-off region and thus influences the power operation of the device. The introduction of the avalanche breakdown mechanism in our model by a completely physical process [13] leads to a significant complication of the computer program. Hence, we have introduced the avalanche breakdown in an empirical manner. First, we measure the avalanche breakdown characteristics of a real MESFET using pulsed bias voltages [15]. Second, we make a computer file with these data on the avalanche breakdown and we model the real transistor. The use of the avalanche breakdown data in our simulation is accomplished by injecting into the device the avalanche current as a function of drain–source and gate–source voltages; an additional factor introduces the avalanche delay. In Fig. 3 we demonstrate the output static characteristics of a real transistor along with the results of the static version of the model and by using the measured data for the avalanche breakdown current.

Another important feature that a dynamic model must take into account is the influence of the parasitic elements. In fact, the presence of parasitic elements in X-band operation is very important, in particular the feedback elements, which, for the usual values of power MESFET's, can transfer power from input to output with considerable gain degradation. In addition, the parasitic elements contribute to a drastic transformation of impedance from the intrinsic transistor output plane to the external impedance plane.

Fig. 4 gives the circuit we have used in order to take into account the parasitic elements. The capacitances C'_{gd}, C'_{gs}, and C'_{ds} are due to the electric coupling between the electrode metallizations, and the capacitances C_g, C_x, and C_d are due to the transistor fixture.

The structure of the computer program, in its dynamic version, is an iterative process that is based on a prediction of gate voltage and source current waveforms ($V_{gs}(t)$ and $I_s(t)$, respectively). At the completion of the computational process for the intrinsic device, we obtain the drain-source voltage $V_{ds}(t)$, the drain current $I_d(t)$, the gate current $I_g(t)$ waveforms, and, consequently, the load impedance Z_L. Then we return to the $I_s(t)$ and $V_{gs}(t)$ waveforms and we perform the appropriate corrections in order to converge towards a desired load impedance, as shown in Fig. 5.

More analytically, Fig. 6 demonstrates the complete flowchart diagram of our model. In this figure we can see that the calculations for the intrinsic device are followed by a Fourier analysis of the total terminal signals $V_{ds}(t)$, $I_d(t)$, and $I_g(t)$. The next step is to take into account the parasitic elements and thus we obtain the input power P_e, the output power P_s, and the external load impedance $Z_{L\,\mathrm{ext}}$. Then, with the terminal signal corrections we test also the bias conditions and we proceed to proper corrections of the drain dc current (I_{d0}), in order to approach the desired drain–source dc voltage (V_{ds0}).

The described computing structure permits a great deal of "freedom" for the simulated systems, but by avoiding

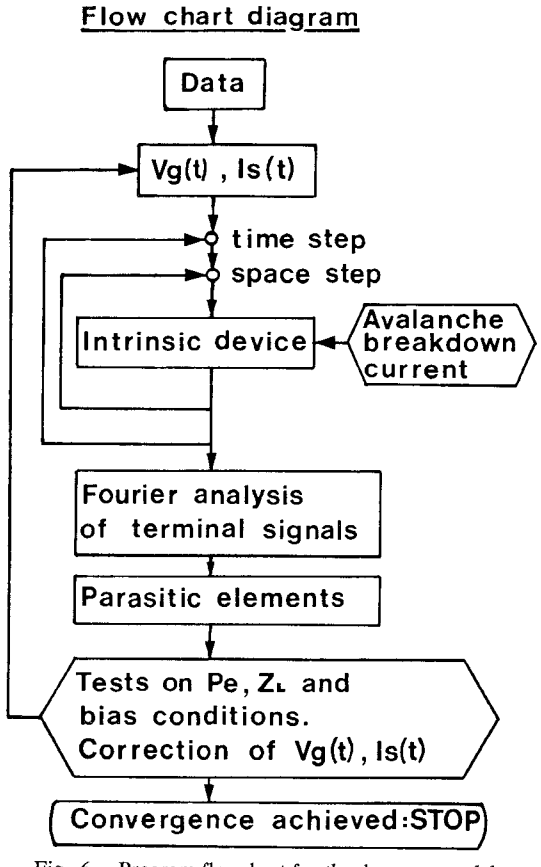

Fig. 6. Program flowchart for the dynamic model

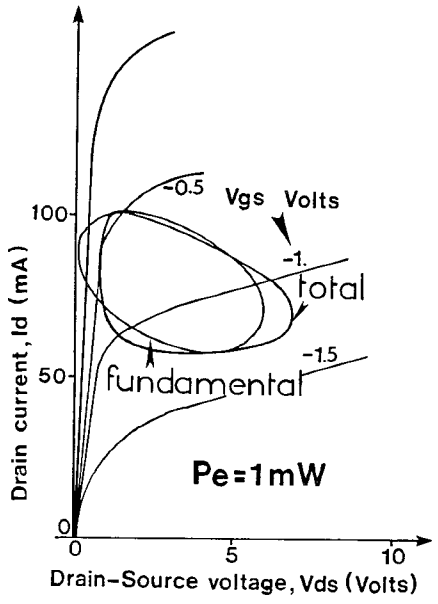

Fig. 7. Dynamic diagram of operation for an input power $P_e = 1$ mW, a drain–source bias voltage $V_{ds0} = 3$ V, and a gate–source bias voltage $V_{g0} = -0.9$ V. (In Figs. 7–10 and 13–16 the ellipses represent the fundamental and the loop the total output signal at the intrinsic drain–source plane. All these diagrams correspond to the matching conditions.)

supplementary external "forcing" conditions our approach becomes more "reliable." The convergence of the system is an *a posteriori* proof of its reliability, even if the above procedure extends the computational time. Hence, scanning systematically the Smith chart for the load impedance under constant input power, we can obtain the matching load impedances for given bias conditions.

Finally, we should emphasize that our dynamic model describes "directly" the physics of the dynamic operation of the device; we do not have to simulate the static $I-V$ characteristics in order to proceed in the simulation of the dynamic operation of the device.

The results of the numerical simulations are presented for a sample with the following characteristics: the doping level is $N_d = 1.6 \times 10^{17}\,\mathrm{cm}^{-3}$ and the thickness of the active layer is $a = 0.15$ μm. The recessed gate (800 Å of recess depth) with a 1 μm $\times$ 600 μm geometry was fabricated by employing Al as gate metal; drain and source ohmic contacts are alloyed Au/Ge with a 5 μm separation and are placed on the top of n^+ layers fabricated by ion implantation.

III. Theoretical and Experimental Results

In this section we shall investigate the influence of the hard limits in large-signal operation in order to understand the different mechanisms involved in this type of operation and consequently determine the power performance of the MESFET's. Basically, we shall study the consequences of the low voltage limit (i.e., the knee voltage) and of the large voltage limit (i.e., breakdown voltage) in large-signal X-band operation and we shall try to draw conclusions about the nature of the optimally matched load impedance at these frequencies.

An additional advantage of our model is its ability to take into account the nonlinearities that are responsible for the production of the upper harmonic components on the output signal. This aspect is very interesting and holds promise for original observations. First, we start from the knee voltage limitation and we continue with the breakdown voltage one. We conclude with a synthesis about the global behavior of power MESFET's.

A. Low Voltage Limitation

In order to set the region of the dynamic operation of the device near the knee voltage region and thus to be able to investigate the consequences of that limitation without the involvement of the other hard limits, we choose a small source–drain bias voltage V_{ds0}. Hence, the device is biased at $V_{ds0} = 3$ V and at a dc gate voltage $V_{g0} = -0.9$ V, which corresponds to a dc drain current of approximately $I_{dss}/2$. Then we impose different levels of input power and we observe the changes in the device behavior.

Figs. 7, 8, 9, and 10 show the dynamic diagrams of operation derived from the numerical simulation for four different input power levels (1, 5, 10, and 15 mW, respectively). For all these cases the output matching conditions are achieved under the above bias conditions. The ellipses in these figures must correspond to the fundamental frequency of 10 GHz. We must emphasize that the dynamic diagrams of operation refer to the intrinsic transistor's output plane, while the external plane load impedances ($Z_{L\,\mathrm{ext}}$) are very different, as can be seen from Table I

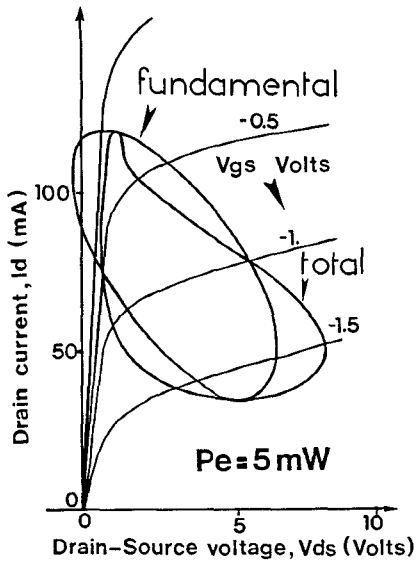

Fig. 8. Dynamic diagram of operation for $P_e = 5$ mW, $V_{ds0} = 3$ V, and $V_{g0} = -0.9$ V.

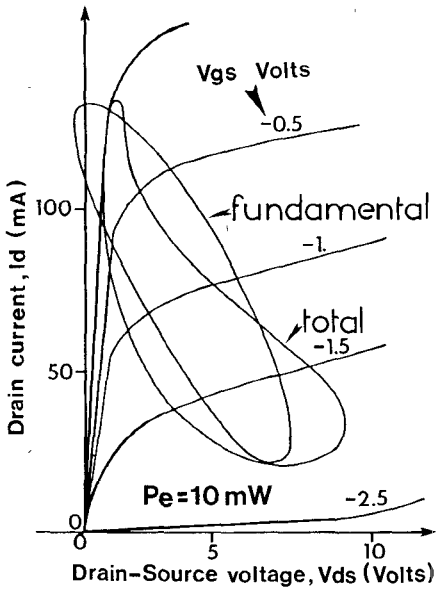

Fig. 9. Dynamic diagram of operation for $P_e = 10$ mW, $V_{ds0} = 3$ V, and $V_{g0} = -0.9$ V.

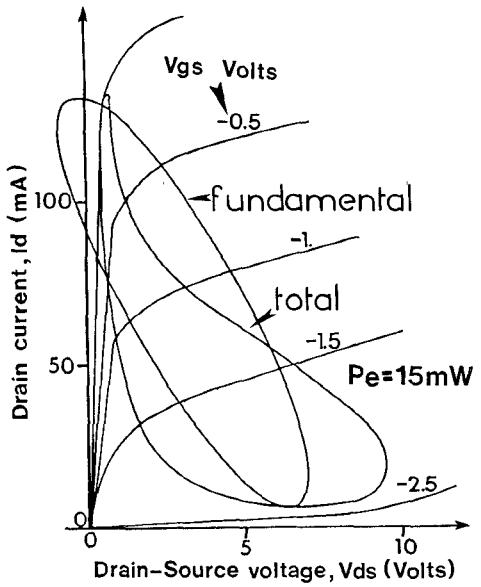

Fig. 10. Dynamic diagram of operation for $P_e = 15$ mW, $V_{ds0} = 3$ V, and $V_{g0} = -0.9$ V.

TABLE I
RESULTS OF THE NUMERICAL SIMULATIONS FOR DIFFERENT INPUT POWER LEVELS

P_e/mW	P_s/mW	Z_{Lext}/Ohms	Z_{Ltr}/Ohms	I_{do}/mA
1	14.3	15+j*35	60+j*123	79
5	51.0	25+j*15	52+j*57	77
10	85.8	35+j*5	54+j*31	75
15	111.0	35+j*5	54+j*31	66

TABLE II
EXPERIMENTAL RESULTS OBTAINED WITH THE LOAD-PULL METHOD [8]

P_e/mW	P_s/mW	Z_{Lext}/Ohms	Z_{Ltr}/Ohms	I_{do}/mA
1.2	5.5	16+j*14	32+j*65	67
4.7	19.2	18+j*9	32+j*55	64
18.6	58.7	16+j*2	27+j*44	57
29.5	81.2	13+j*1	29+j*42	54
46.8	104.7	20-j*2	31+j*36	54

(Z_{Ltr} is the load impedance at the intrinsic transistor plane). Note that we have imposed an open circuit for the harmonic components of the output signal but we shall comment later on this point (see subsection B).

Table II contains the experimental results obtained with the load-pull method.

Observation of these results leads to the conclusion that the limitation of the knee voltage V_{dt} has a drastic role, even for a relatively small power level. One can observe from the above figures that for a small power level the ellipses, which correspond to the fundamental frequency, are "very inclined" (i.e., the angle θ is small) and occupy a relatively large area in the $I_{ds}-V_{ds}$ output characteristic plane. As the power increases the output signal "touches" more and more the limit of the knee voltage and this has as a consequence the clipping of the output signal. (In the present case only the output voltage distortion take place because we have imposed an open circuit for the upper harmonics.)

It is interesting to note the extension of the fundamental component of the output voltage beyond the static output characteristic frame, which signifies that a behavior of the "Snider kind" can effectively occur.

Such behavior requires the presence of upper harmonic components in order to keep the total dynamic diagram of operation completely within the frame of $I_{ds}-V_{ds}$ static characteristics. Furthermore, we must inquire whether this effect can result in an output power higher than the output power obtained with a conventional class A load resistance.

When the dynamic diagram of operation reaches the hard limit of the knee voltage, any supplementary augmentation of the input power results in an extension of the fundamental component of the output voltage beyond the static output characteristic frame. However, this effect, which is initially beneficial to the output power, finally affects the power gain.

Indeed, as the input power is increased the onset of the clipping of the output signal leads to a degradation of the power gain, as explained below. Hence, since the output voltage swing was limited by the knee voltage, an alternative solution emerges naturally for the device: the exploitation of the output current swing which is not yet limited. This change from a situation of a "privileged" voltage swing to another which "privileges" the current swing corresponds to the restoration of the dynamic diagram of operation (i.e., the augmentation of the angle θ in Fig. 1). Hence, with the restoration of the dynamic diagram of operation the increase in output power is due to the exploitation of the output current swing from the pinch-off to I_{dss}.

Therefore, this passage from a situation of "voltage swing" to another of "current swing" characterizes the output matching under large-signal conditions and thus differs from the small-signal matching.

This process of dynamic diagram restoration as the power level increases is carried out to avoid the clipping of the output signal, which influences the swing of the output voltage and thus limits the output power. On the other hand the clipping modifies the output signal and changes the feedback conditions (mainly through the parasitic elements) and degrades the power gain.

These two actions are translated as output power compression. Unfortunately, the passage from the "voltage swing" to the "current swing" mode of operation does not take place without exacting a price because we keep away from the small-signal matching conditions. Although we avoid clipping of the output signal, we observe an output power compression due to the output mismatching in comparison with the small-signal matching.

Finally, the large-signal matching is a compromise between these contradictory situations.

The experimental results, presented in Table II, show that the real MESFET behaves in a manner similar to the simulated one. Hence, as the power level increases the load matched impedance changes (mainly through the change of the reactance) in order to provide a better exploitation of the current swing instead of the voltage swing. The compression of the output power is a natural consequence of this evolution, according to the previous analysis.

The differences between the experimental results and those of the numerical simulations, mainly on the power gain values, could be attributed to the uncertainties that underlie the measured values of the parasitic elements. In fact, the power gain of the transistors at X-band frequencies is very sensitive to the values of the feedback parasitic elements.

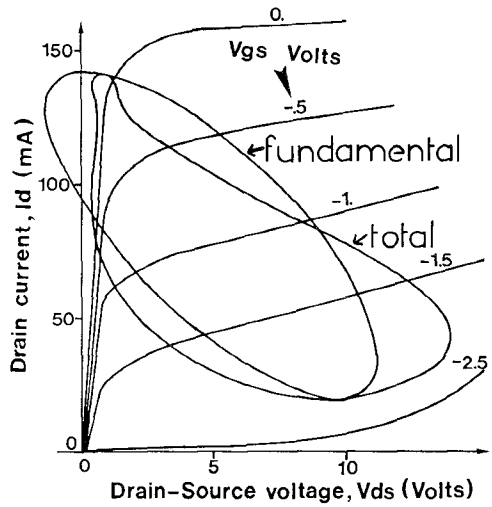

Fig. 11. Dynamic diagram of operation for $P_e = 15$ mW, $V_{ds0} = 5$ V, and $V_{g0} = -0.9$ V.

Furthermore, we note that the decrease of bias current (I_{d0}) with power level is due to the dc component of the voltage produced by clipping of the output signal.

Additional indications of the low voltage limitation could be manifested by modifying the source–drain bias voltage V_{ds0} because it would change the relative position of the fundamental limitations of the $I_{ds}-V_{ds}$ output characteristics with respect to the dynamic diagram of operation.

Fig. 11 shows the simulated dynamic diagram of operation for $V_{ds0} = 5$ V and with $V_{g0} = -0.9$ V and $P_e = 15$ mW. Hence, this figure can be compared with Fig. 10.

We have subtracted the avalanche breakdown in the above numerical simulation in order to distinguish the different mechanisms that could influence the behavior of the device.

Thus, we observe that for greater V_{ds0} we obtain better performance in output power, since the output voltage swing has a greater space to exploit with lower signal distortion and this permits the dynamic diagram of operation to be more inclined, i.e., close to small-signal matching conditions. This behavior is in agreement with our previous explanations.

The same type of behavior can be observed in the experimental measurements. Figs. 12 and 13 show the load matching impedance evolution for the real transistor.

With the exception of certain irregularities, the real part R_L and the imaginary part X_L of the load matching impedance are increasing with the source–drain bias voltage. The evolution of X_L is more spectacular and corresponds to the "liberation" of the dynamic diagram of operation from the knee voltage when the bias drain–source voltage increases.

B. The Role of the Upper Harmonic Components

The unavoidable presence of output signal distortion in large-signal operation involves the problem of investigating the load impedances that must be applied to harmonic

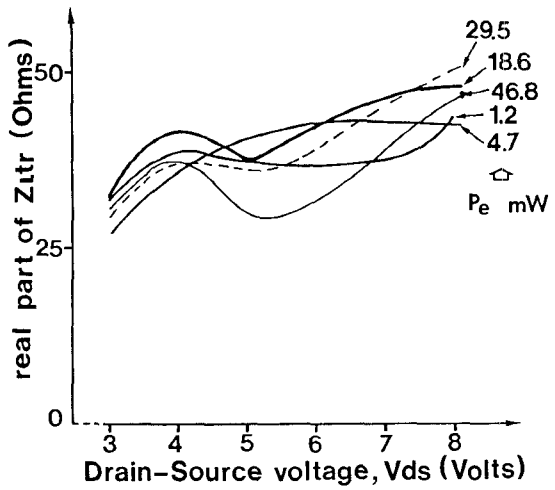

Fig. 12. Experimental evolution of the real part of the matched load impedance ($Z_{L\,tr}$) with the drain–source bias voltage and for different input power levels (P_e). The values of $Z_{L\,tr}$ refer to the drain–source plane of the intrinsic device.

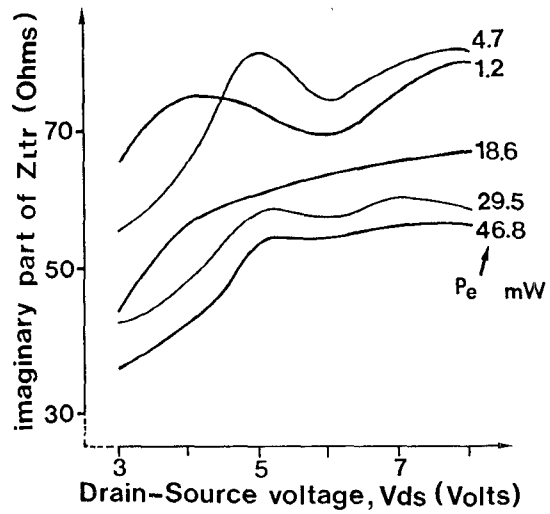

Fig. 13. Experimental evolution of the imaginary part of the matched load impedance ($Z_{L\,tr}$) with the drain–source bias voltage and for different levels of P_e.

frequencies in order to obtain the optimum performance for power operation.

The two extreme cases are the open circuit and the short circuit. In the first case the distortion is present only at the output voltage signal, and in the second it is present only in the output current signal.

From the results discussed in the previous paragraph we can observe that, for a MESFET with the above technological parameters, the required matching load leads to highly inclined dynamic diagrams of operation, which have as a consequence the fact that there is a knee voltage that imposes a limit on signal swing for class A type of operation. However, the presence of harmonic components in the output voltage permits the fundamental frequency signal to surpass the knee voltage limit and, then, to swing closest to small-signal matching conditions.

These qualitative observations lead to the conclusion that the open circuit for the upper harmonic frequencies is beneficial to output power for the above transistor. In fact, the numerical simulation has confirmed this conclusion, but the differences in output power between the open circuit case and any other choice have been small (see Fig. 14).

Nevertheless, we have used the open circuit for all the results discussed in this paper.

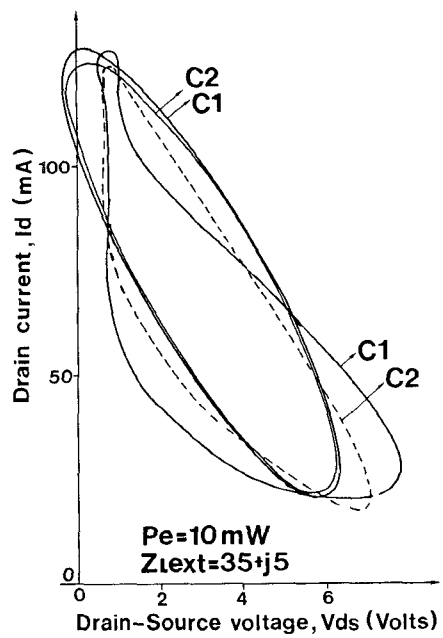

Fig. 14. Dynamic diagram of operation and corresponding ellipses when the impedance at the second harmonic (Z_{2h}) is an open circuit (curves C1) and when $Z_{2h} = 118 - j*52\ \Omega$, $P_e = 10$ mW, and $Z_{L\,ext} = 35 + j*5\ \Omega$ for both cases.

C. High Voltage Limitation

The breakdown voltage is the high limit in voltage on the static output characteristic frame. The importance of avalanche breakdown, especially in power limitation, is well known but the exact function of this physical mechanism is not well understood.

We performed numerical simulations with our model in order to compare the operation of the MESFET under avalanche breakdown conditions and without this physical mechanism. Table III shows the results of some simulations. For all the cases the input power is $P_e = 15$ mW and the bias voltages are $V_{ds0} = 5$ V and $V_{g0} = -0.9$ V. The comparison between the case with and without the breakdown mechanism is established under the same external load impedances ($Z_{L\,ext}$). Also, in Table III we give the values of the load impedance in the drain–source plane (Z_{tran}), the output power delivered at $Z_{L\,ext}(P_s)$, the magnitude of the fundamental component of the gate current ($|I_g|$), and its phase difference with respect to the intrinsic gate–source voltage (ϕ_{Ig}).

These results confirm the common idea that the avalanche breakdown has a destructive effect not only on the device but, when the power level is high, the power

TABLE III
RESULTS OF THE NUMERICAL SIMULATIONS CONCERNING THE INFLUENCE OF THE AVALANCHE BREAKDOWN CURRENTS ($P_e = 15$ mW)

Z_{Lext}/Ohms	Z_{tran}/Ohms	P_s/mW	$\lvert I_g \rvert$/mA	ϕ_{Ig}/deg.
	With avalanche current			
30+j*15	61+j*52	121.9	13.7	82
40+j*15	69+j*37	131.8	12.5	84
50+j*15	79+j*21	121.4	11.7	83
60+j*15	86+j*8	124.6	11.6	79
	Without avalanche current			
30+j*15	61+j*51	157.1	12.4	82
40+j*15	73+j*36	151.2	11.8	91
50+j*15	83+j*21	147.6	11.5	89
60+j*15	83+j*8	125.5	11.4	87

performances of MESFET are degraded. In fact, inspection of the above results shows that the major effect of the breakdown current is on the gate current phase. In the case of the breakdown mechanism this phase changes in a manner that increases the input power and thus degrades the power gain. It is obvious that this change in the phase of the gate current is due to the superposition of the breakdown current on the RF gate voltage as the dynamic diagram of operation traverses the breakdown region.

But when the gate breakdown current increases the condition of fixed input power ($P_e = 15$ mW) imposes a decrease in gate–source RF voltage in order to achieve this fixed P_e. This effect results, finally, in a decrease in output power.

Note that whereas for some cases the ϕ_{Ig} is greater than 90° the input of the global device (i.e., including the parasitic elements) is stable just because of the presence of the parasitic elements. (In other words we have a direct transfer of RF power from the input to the output through the feedback parasitic elements.)

Moreover, for all the above reasons the dynamic diagram of operation "wants" to avoid the breakdown region in the output static characteristics in order to prevent the power gain degradation due to the breakdown phenomenon. An illustration of this physical behavior is presented in Figs. 15 and 16, which show the simulated dynamic diagrams of operation under matching conditions for both cases, with breakdown mechanism and without.

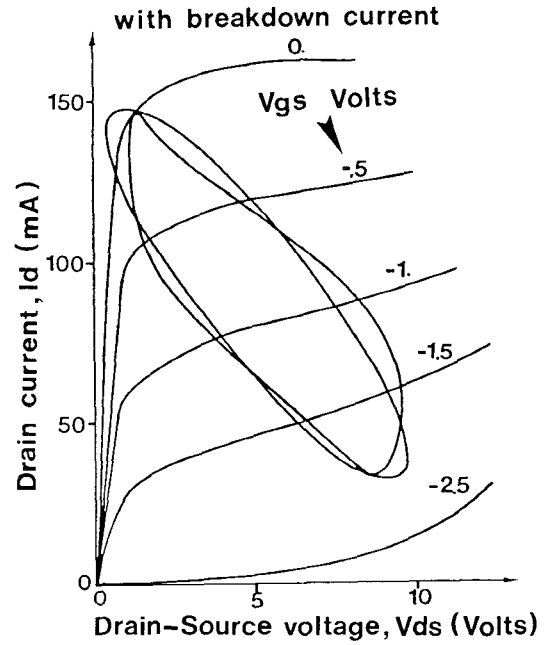

Fig. 15. Dynamic diagram of operation when the avalanche breakdown current is taken into account.

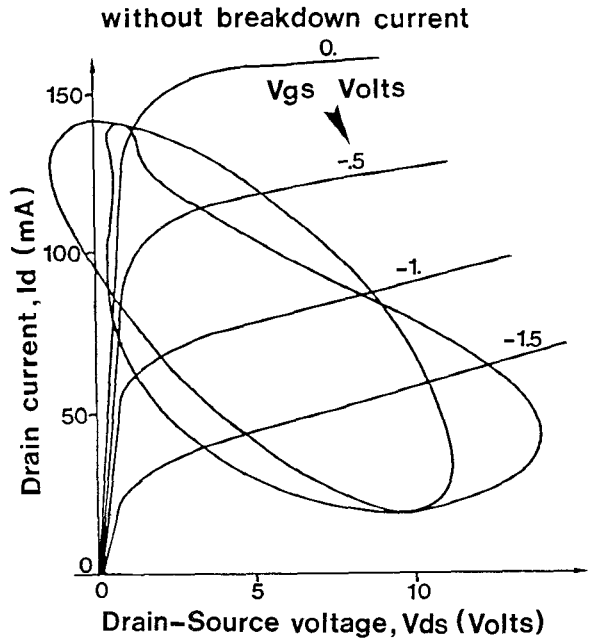

Fig. 16. Dynamic diagram of operation without avalanche breakdown current.

IV. CONCLUSION

In this paper we have investigated the mechanisms that limit the output power of MESFET's at X-band frequencies. We have studied how the knee voltage and the avalanche breakdown determine the large-signal matching load impedances. It is revealed that the matching load impedance is not a resistive load in the output plane of the intrinsic device. Moreover, it was demonstrated that the matching mechanism in large-signal operation is different from the small-signal one. In addition, we have commented on the role of the harmonic components of the output signal. Both the numerical model and the experimental results have confirmed our analysis about the fundamental mechanisms that govern the microwave power operation of the MESFET's.

The theoretical approach of Snider [4], according to which we can obtain, from an overdriven power amplifier, an output power that exceeds the maximum available power of classic class A operation, is unrealistic for X-band power MESFET operation. This limitation of output power is related to power gain degradation in large-signal operation.

For maximum output power it is not sufficient to have a high breakdown voltage without the satisfaction of the

other requirement, namely that of small-signal matching impedance (i.e., the complex conjugate of the output impedance of the device) being close to classic class A load. For these reasons, let us emphasize at the end of this paper that the greater the importance of the small-signal power gain of MESFET's, the greater the risk of a premature power gain compression. This last point is very essential when one has to make the appropriate technological choices for maximum output power.

ACKNOWLEDGMENT

The authors wish to thank A. Cappy and R. Wroblewski for their helpful discussions and advice.

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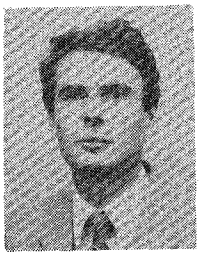

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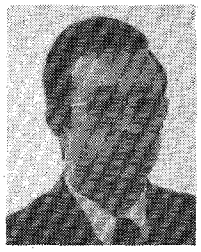

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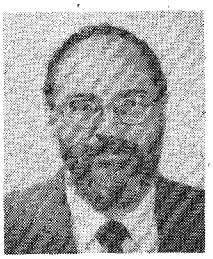

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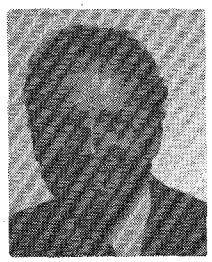

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